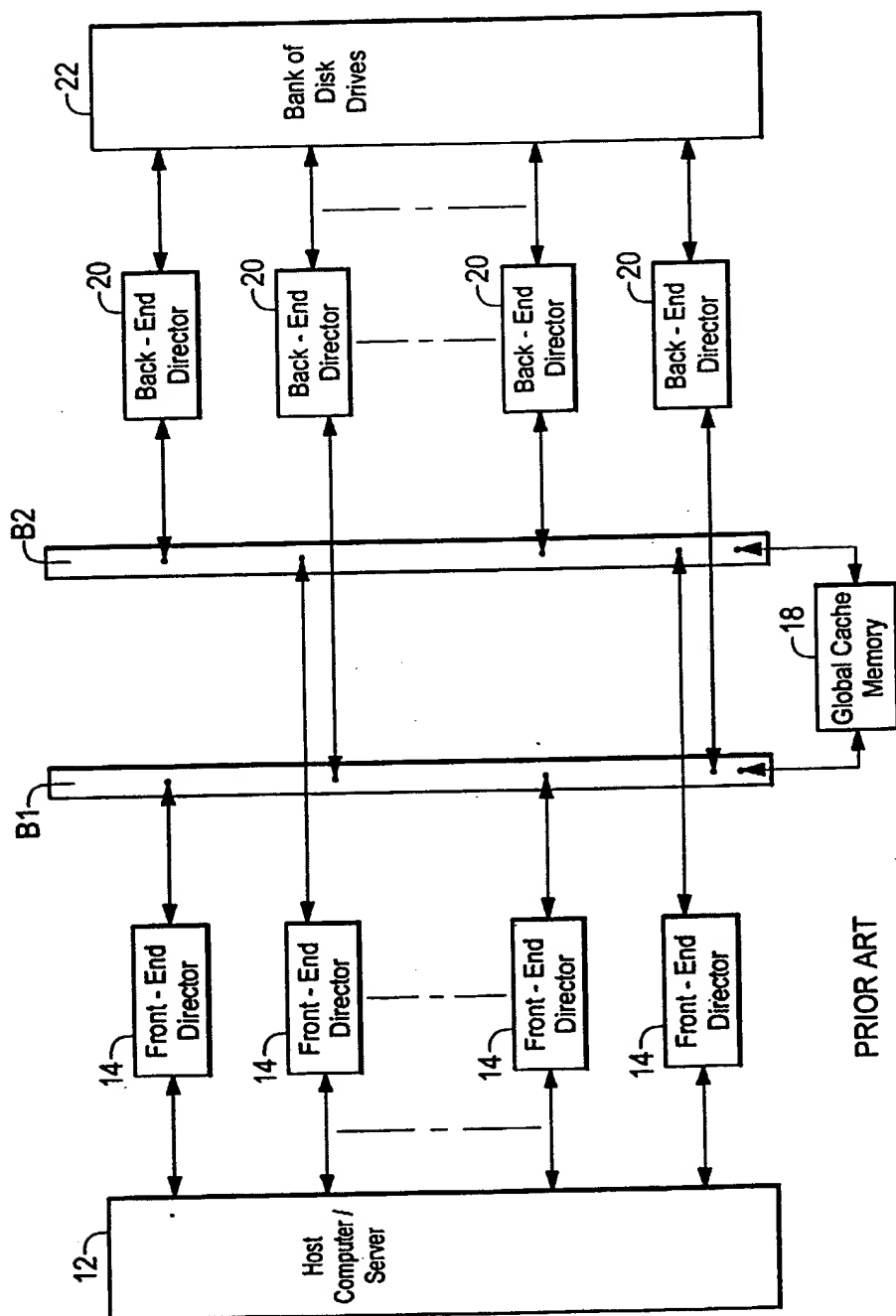


1/25



PRIOR ART

**FIG. 1**

2/25

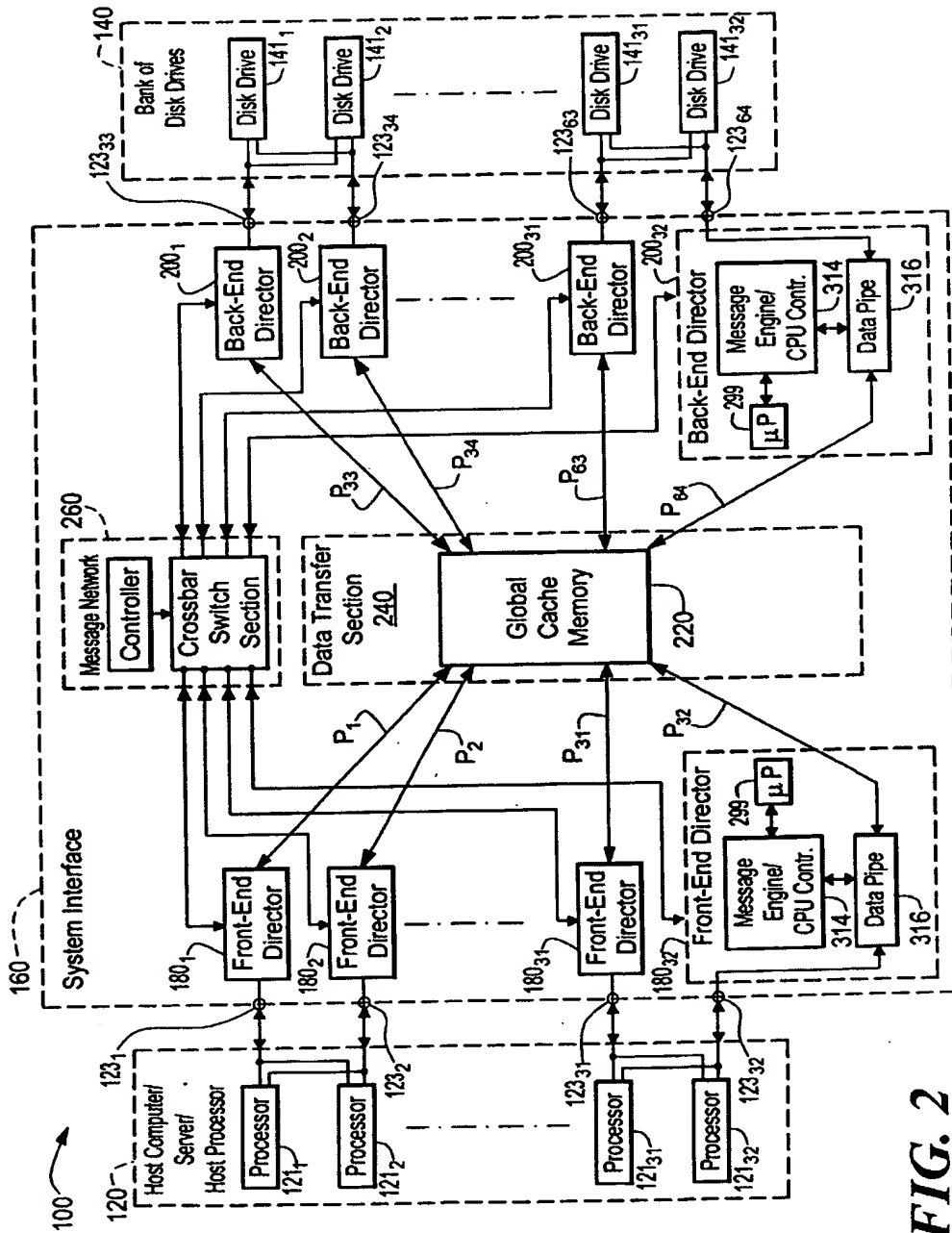
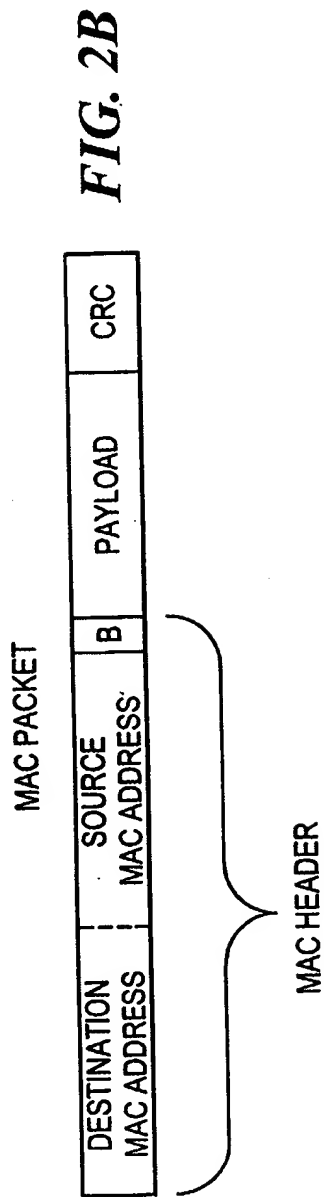
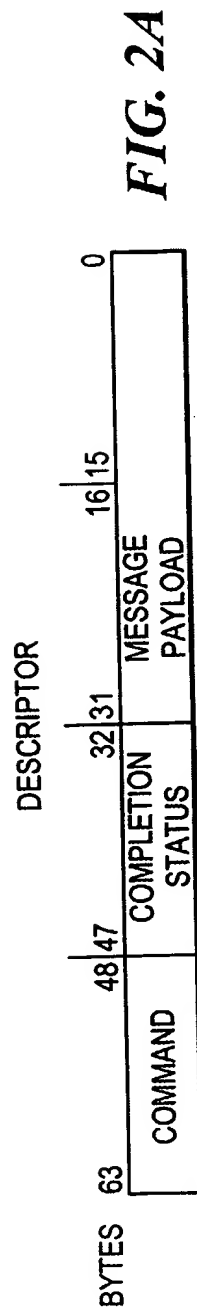


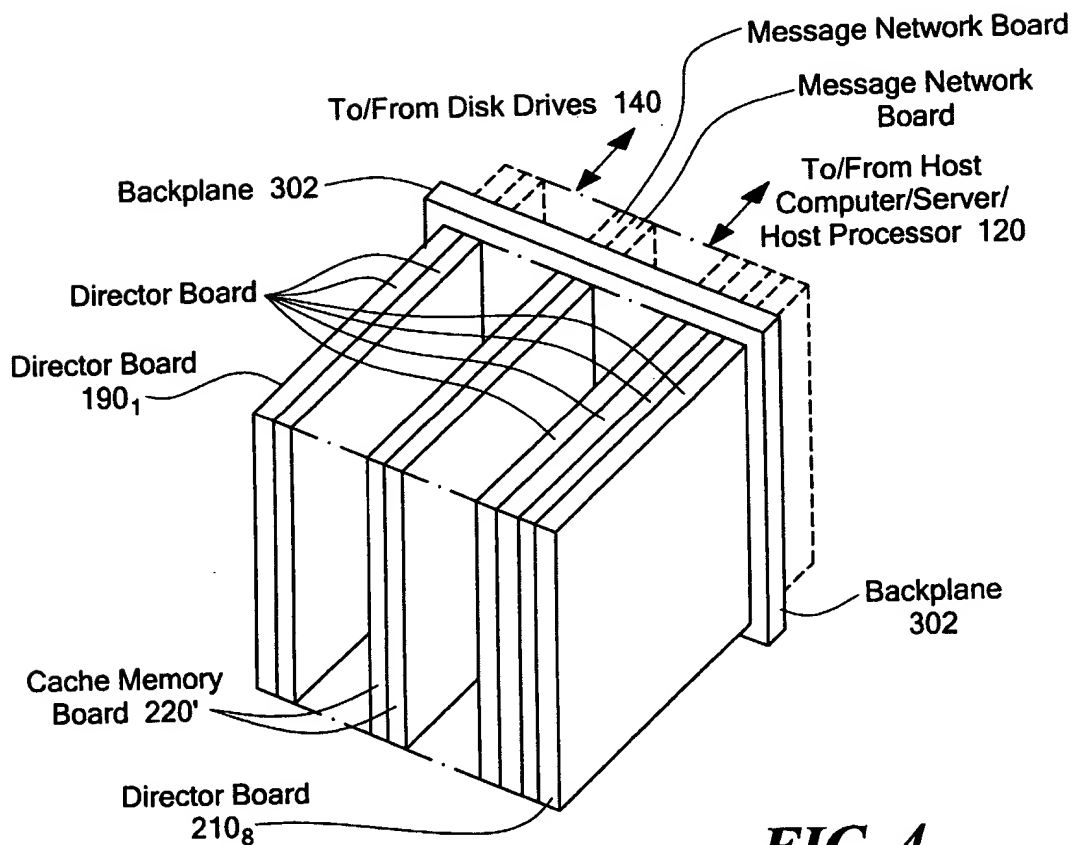
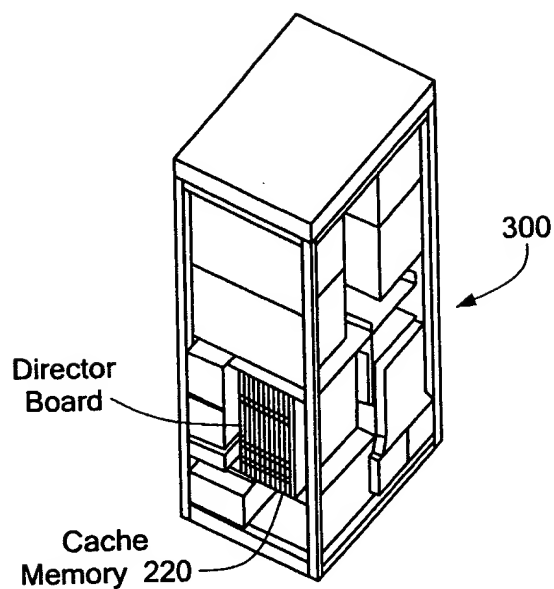
FIG. 2

3/25



4/25

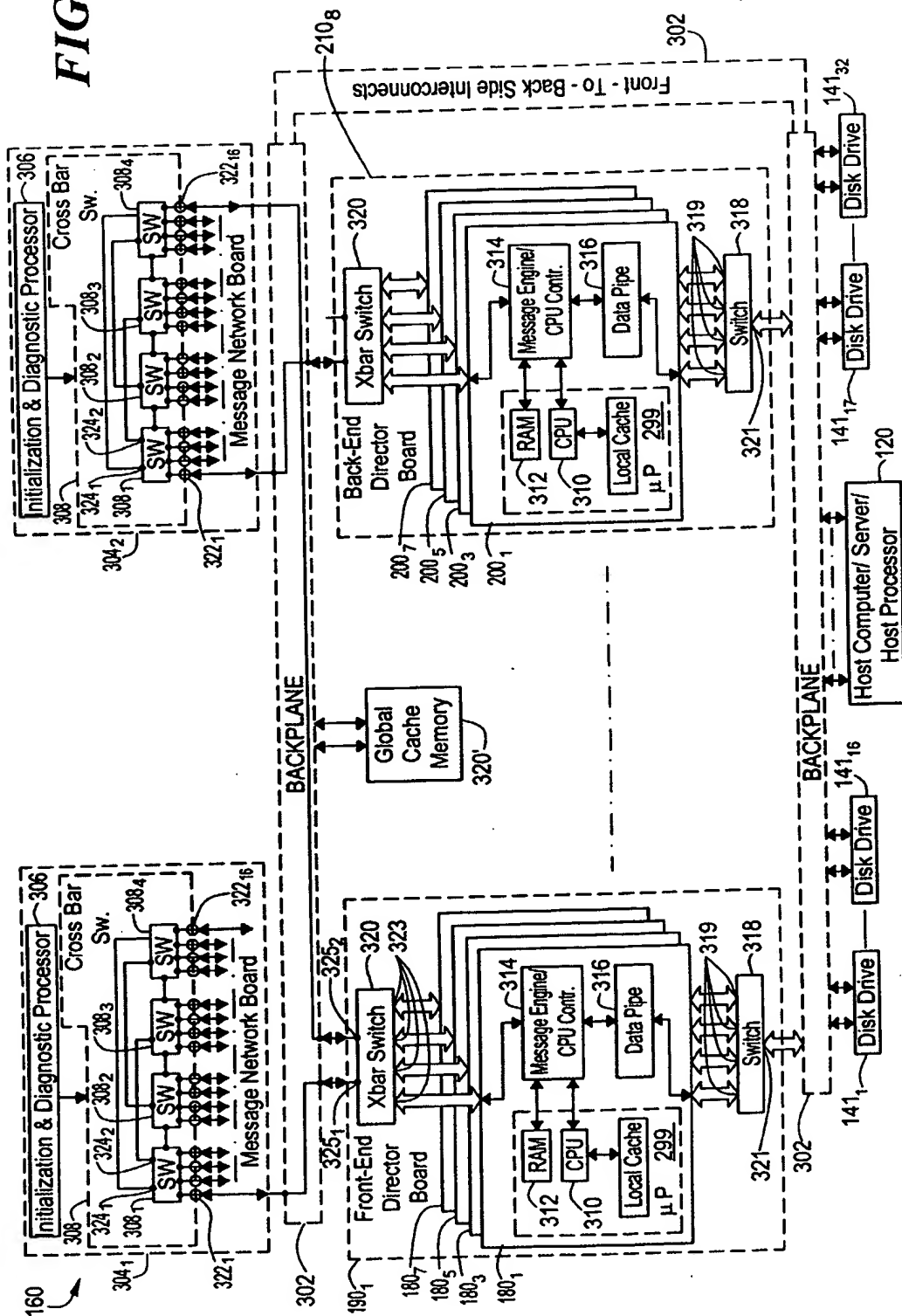
**FIG. 3**



**FIG. 4**

5/25

FIG. 5



6/25

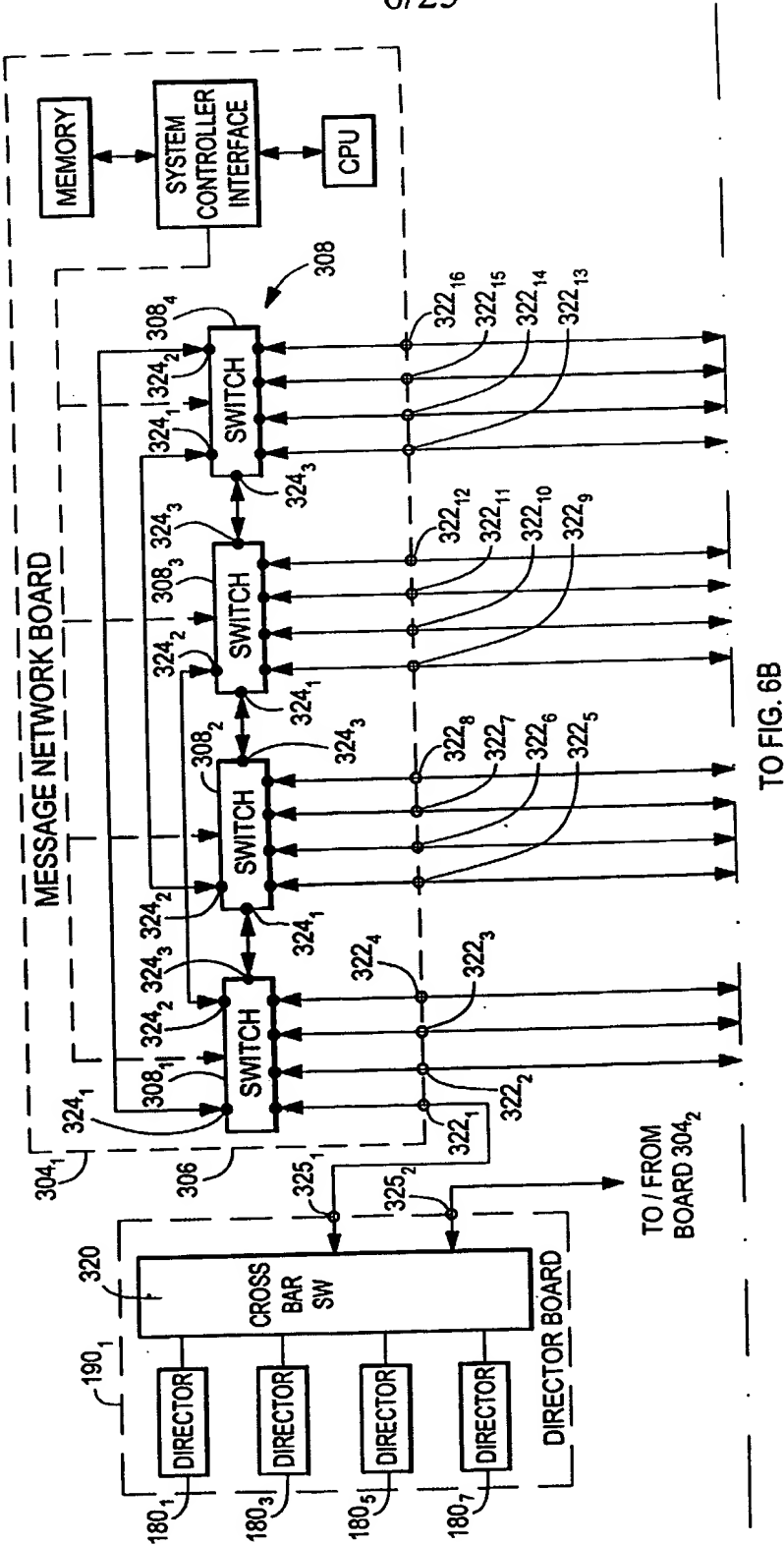


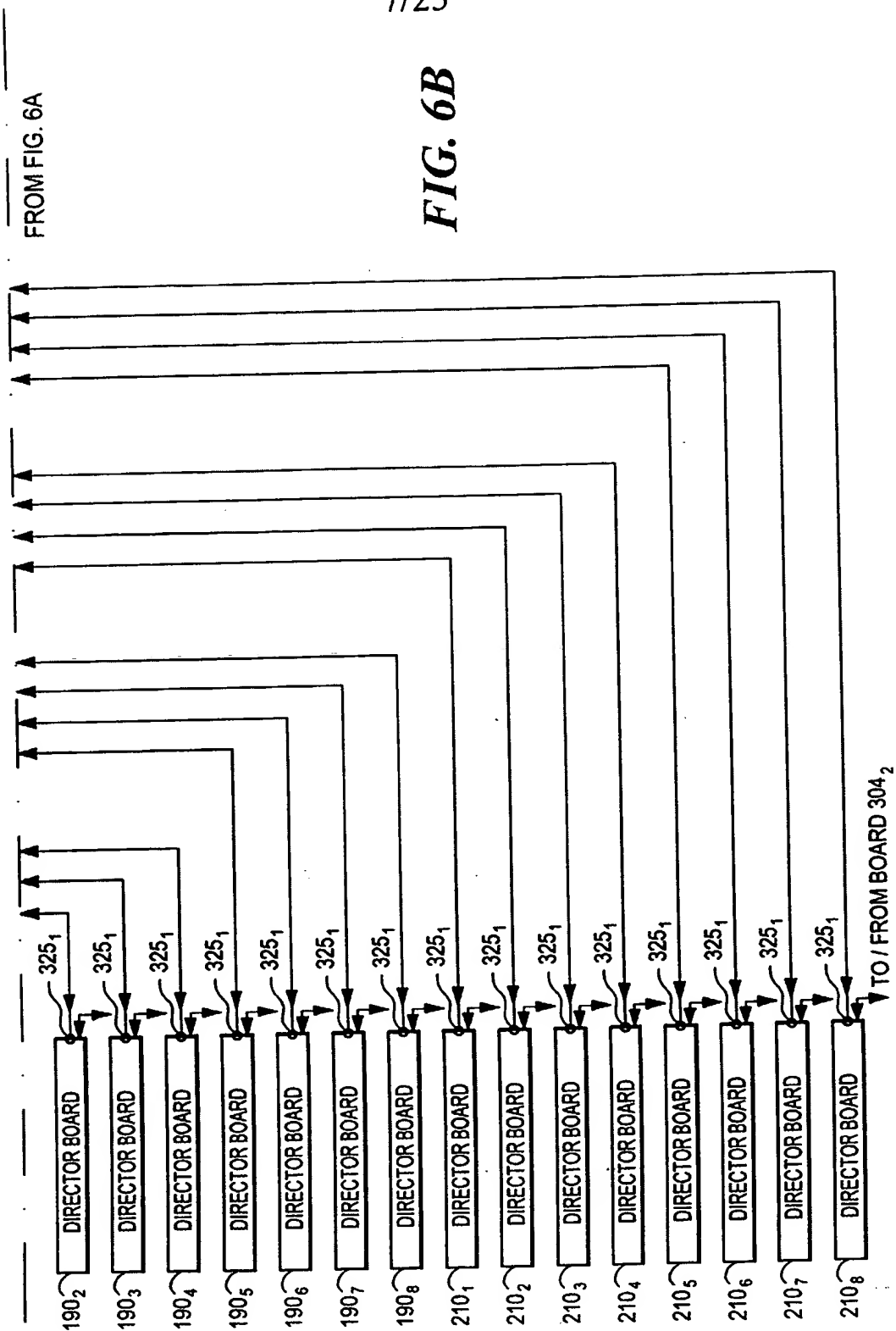
FIG. 6A

FIG. 6A
FIG. 6B

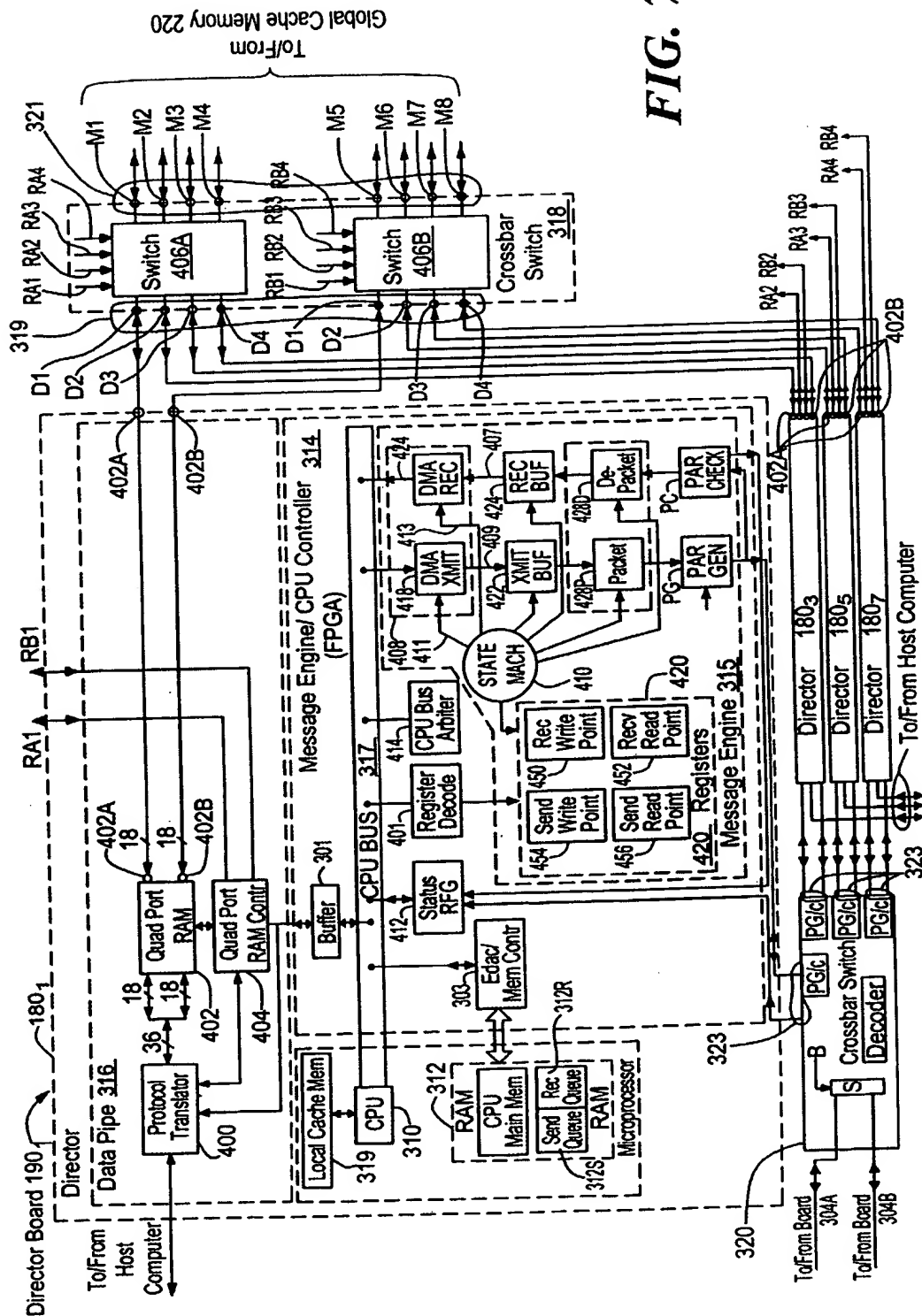
FIG. 6

7/25

FIG. 6B

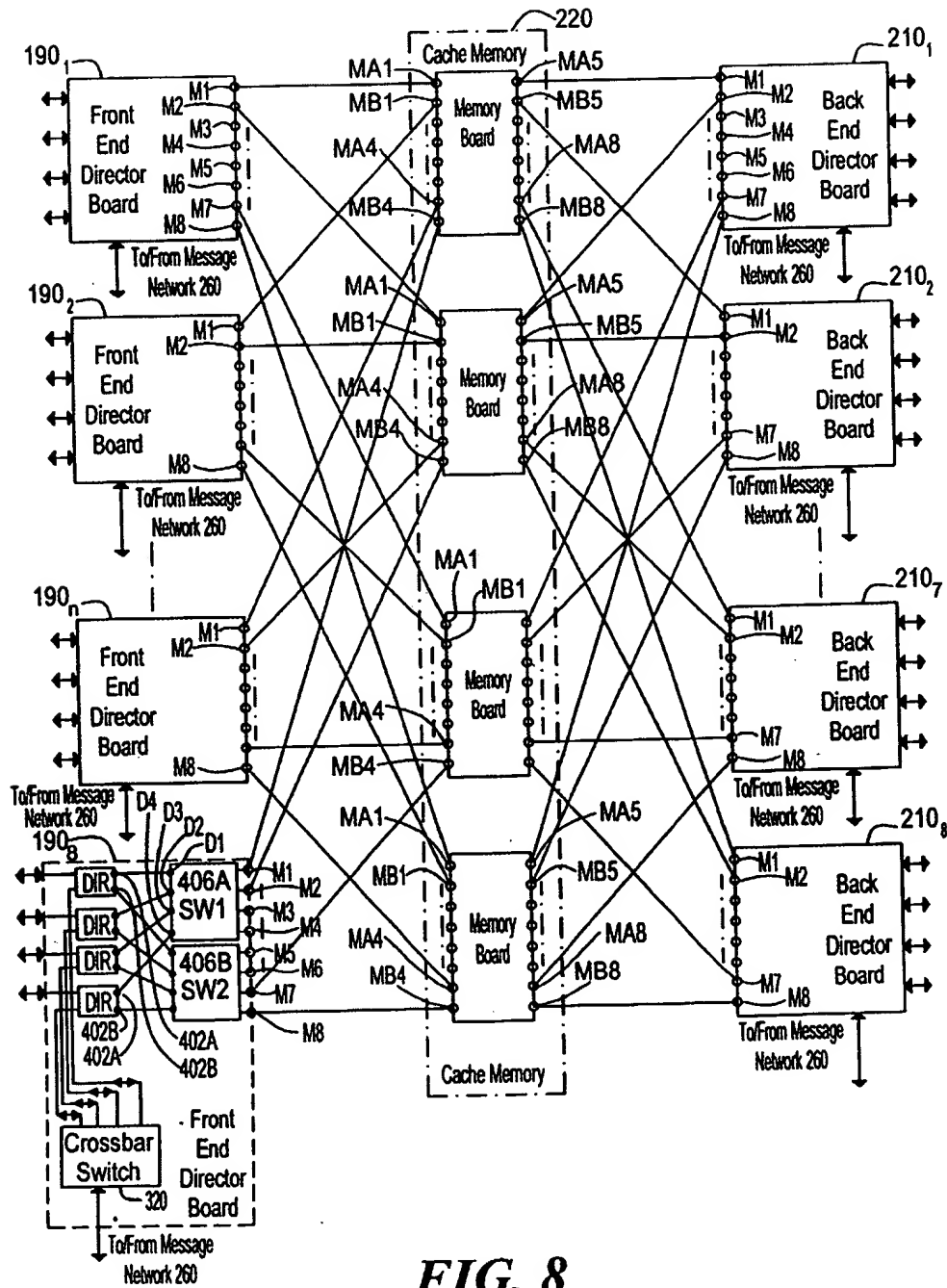


**FIG. 7**





9/25



**FIG. 8**

10/25

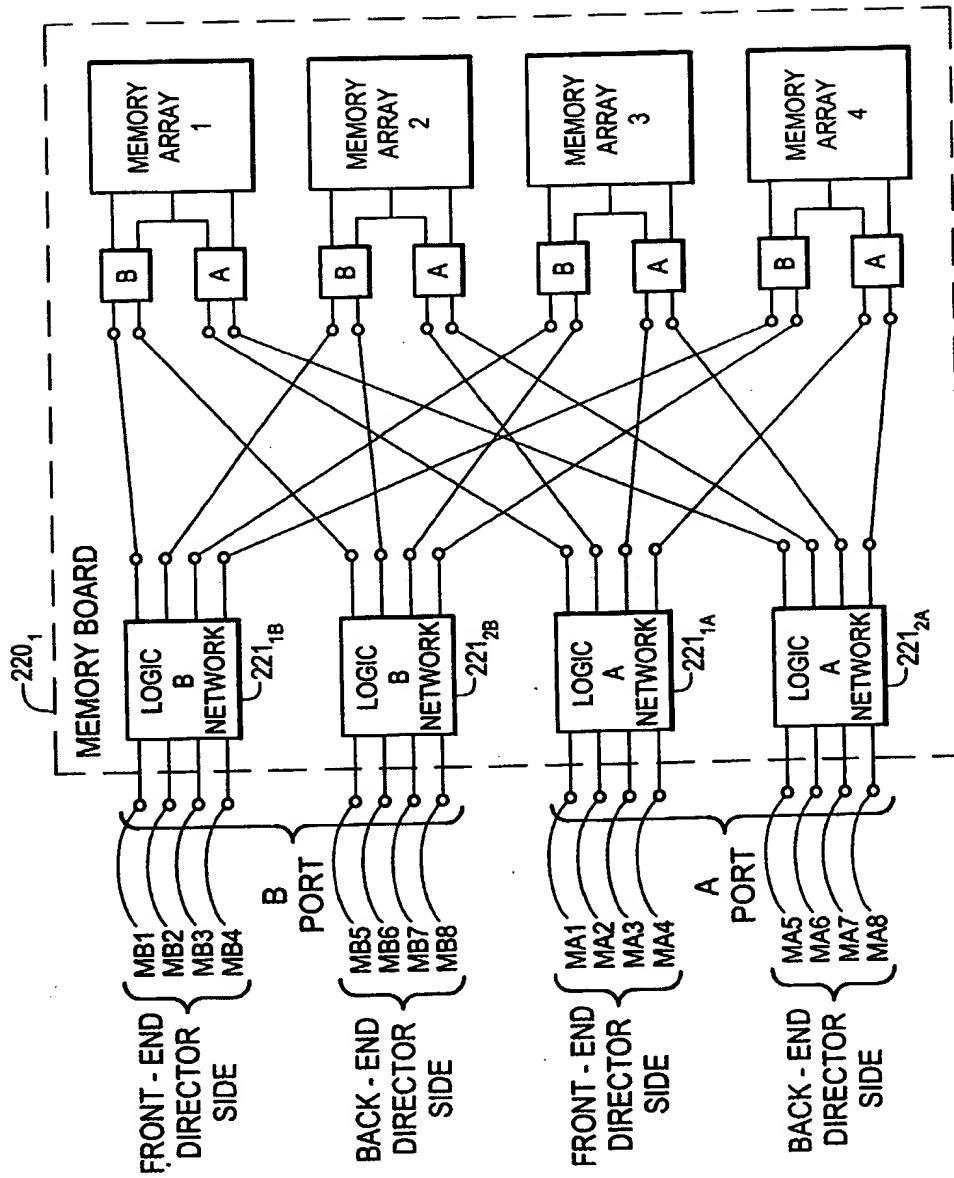
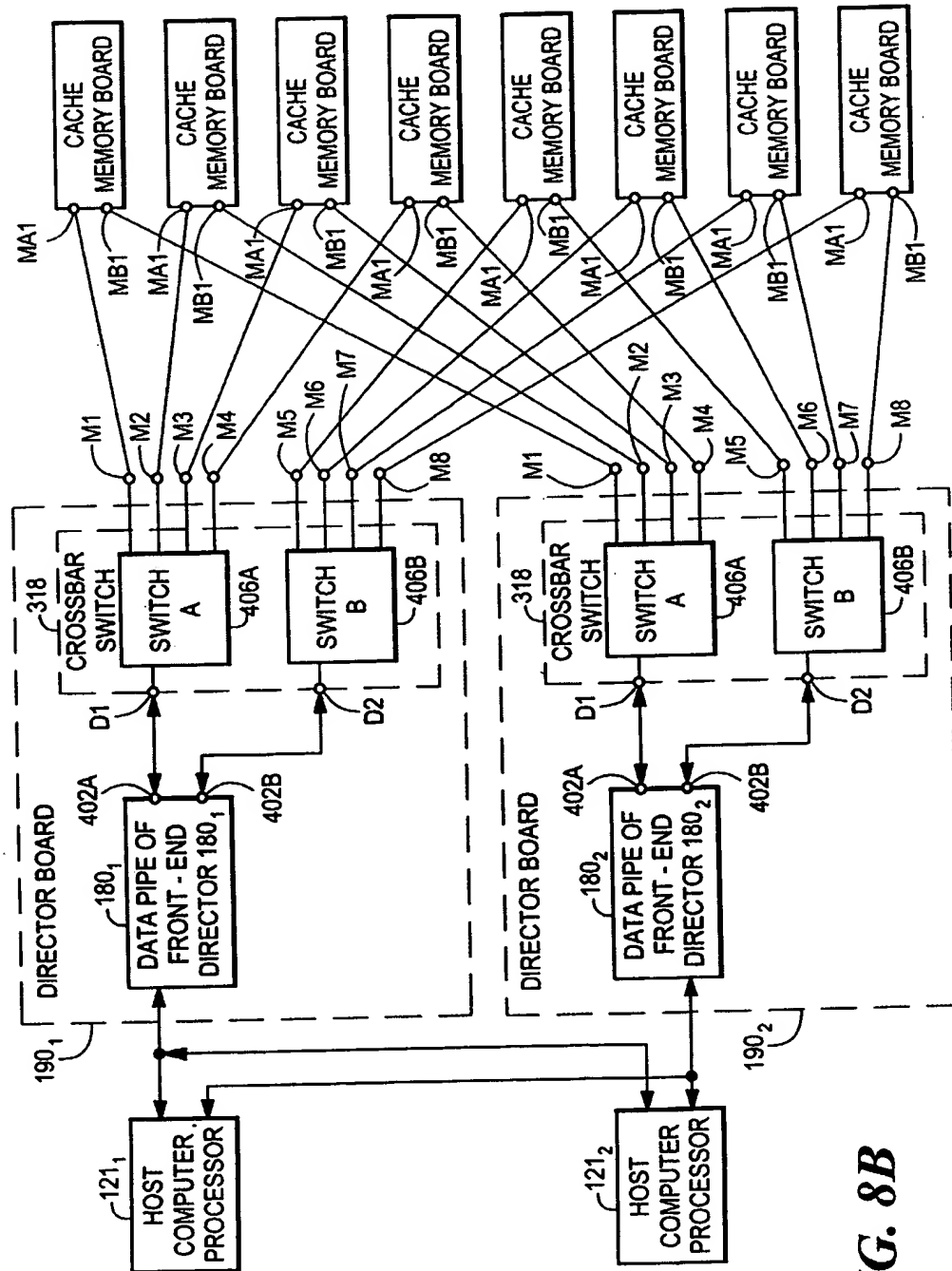


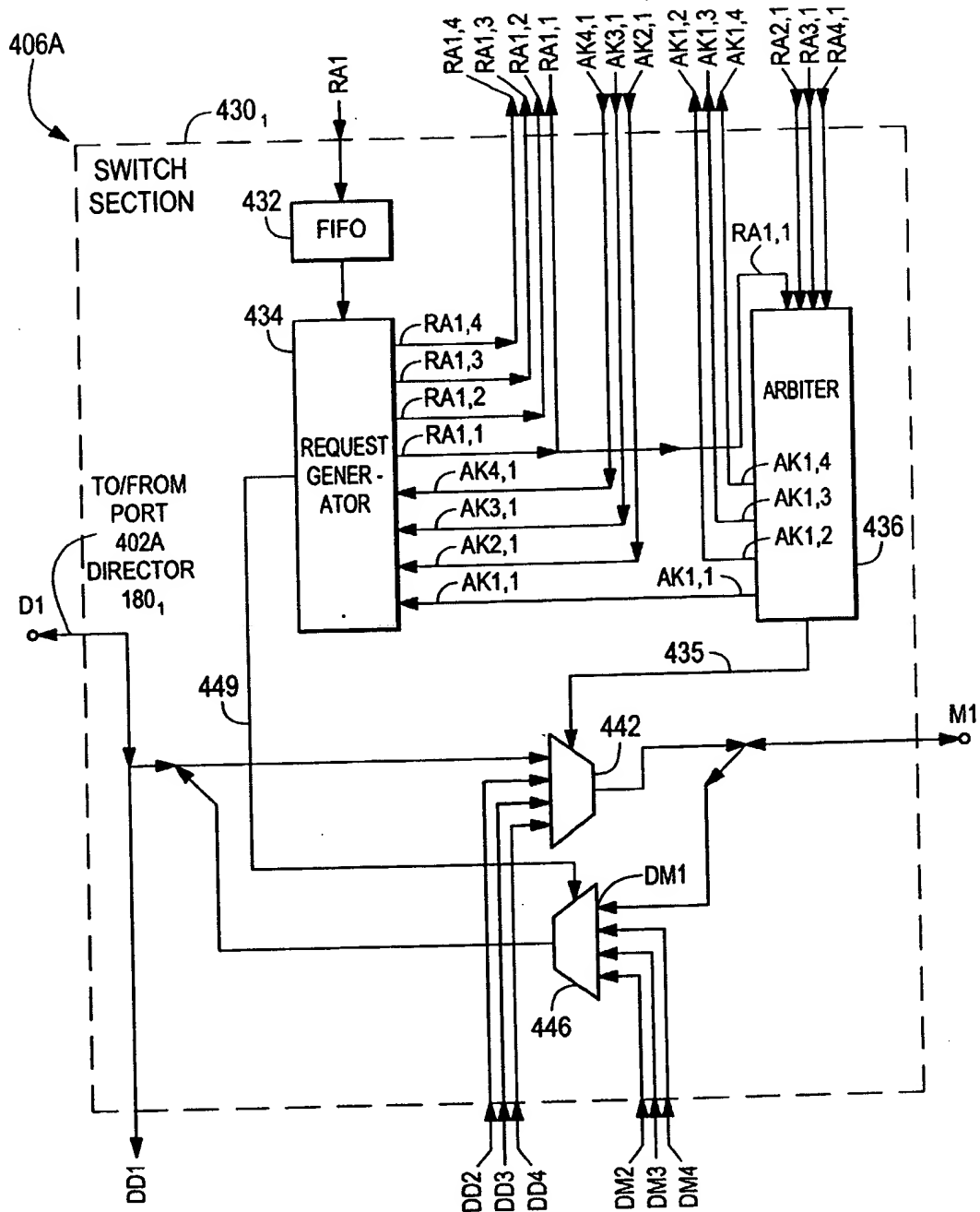
FIG. 8A

11/25



**FIG. 8B**

12/25



**FIG. 8C-1**

**FIG. 8C**

FIG. 8C-1
FIG. 8C-2

13/25

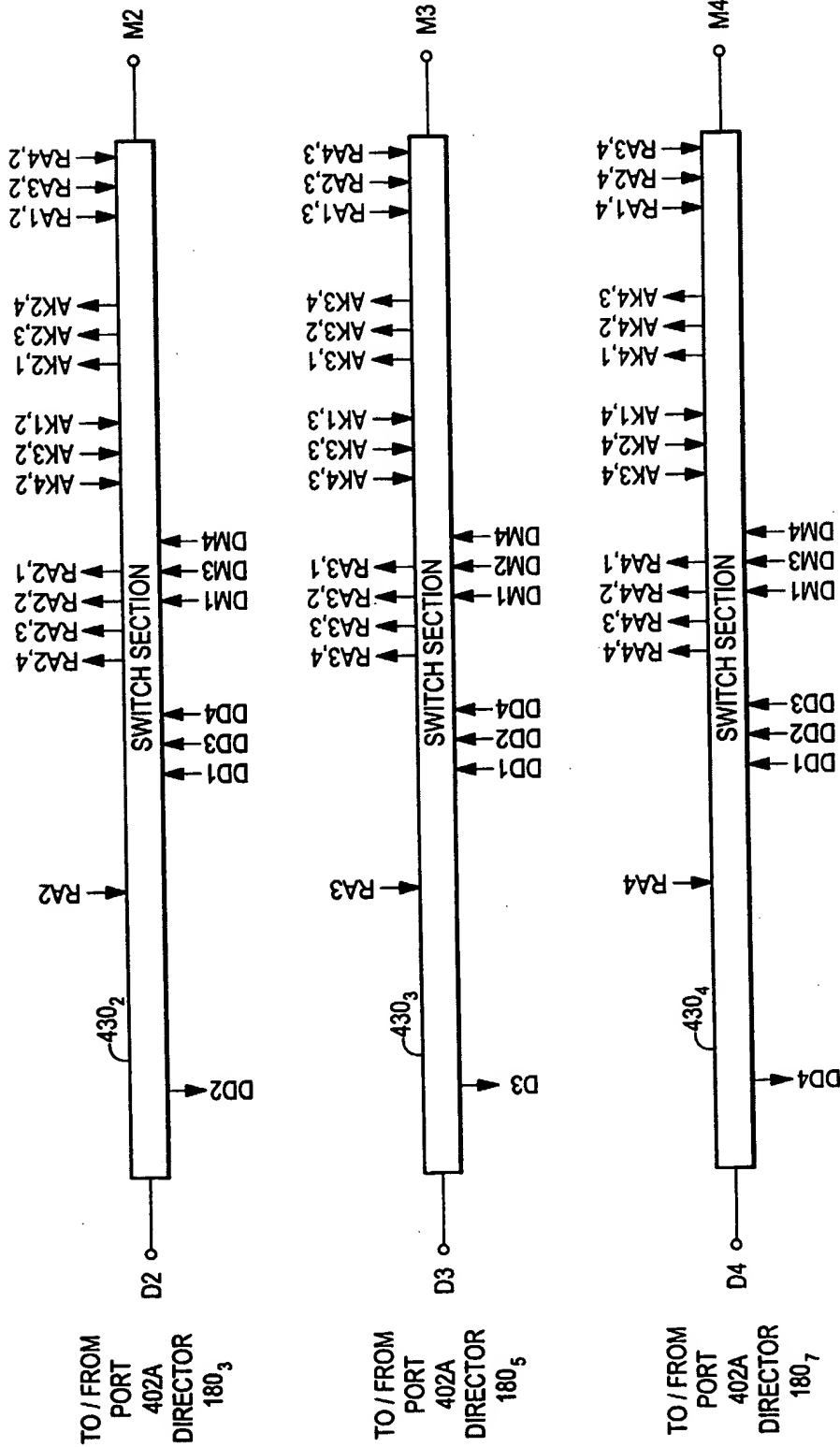


FIG. 8C-2



**FIG. 9**

15/25

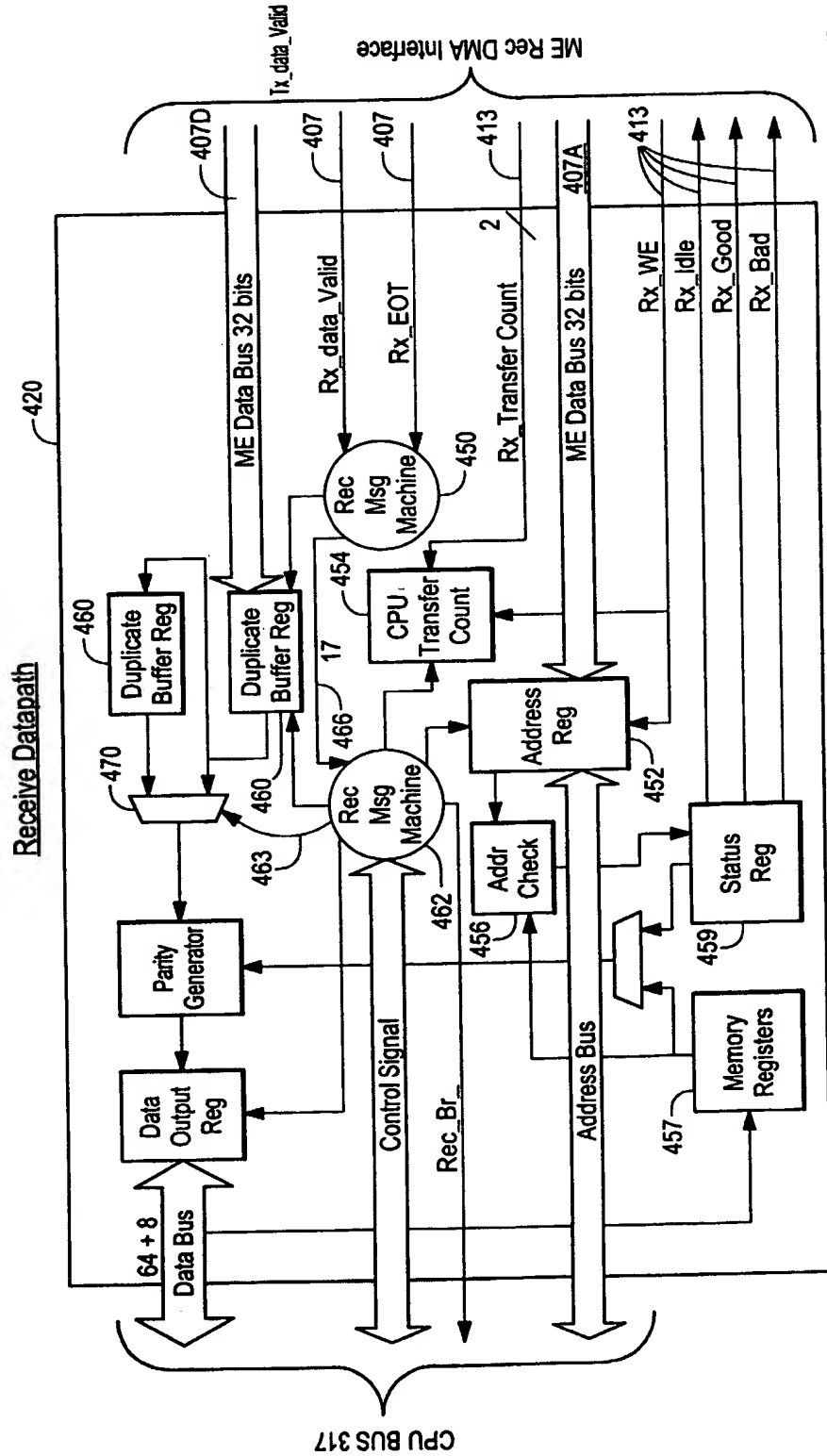
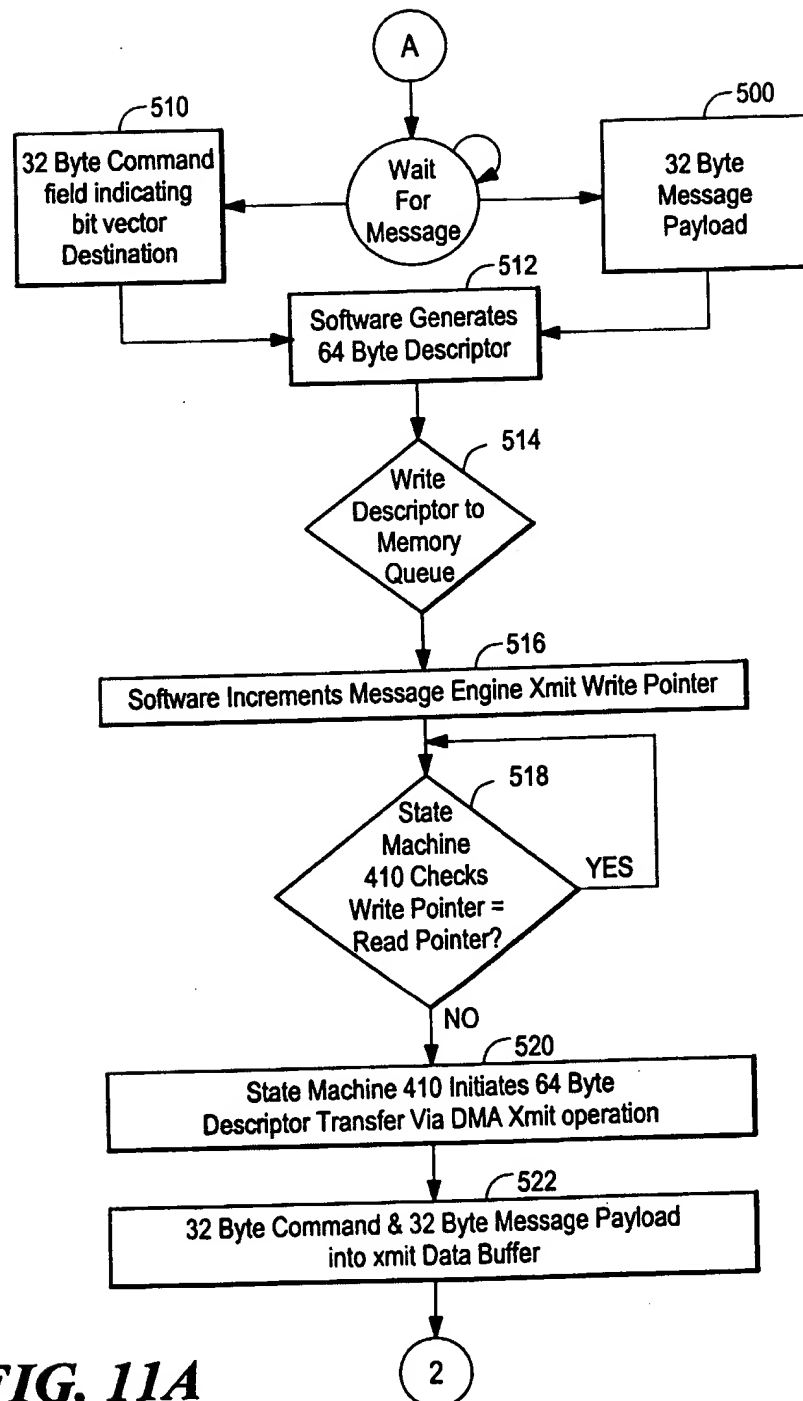
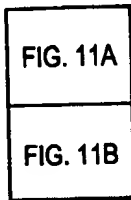


FIG. 10

16/25

**FIG. 11**

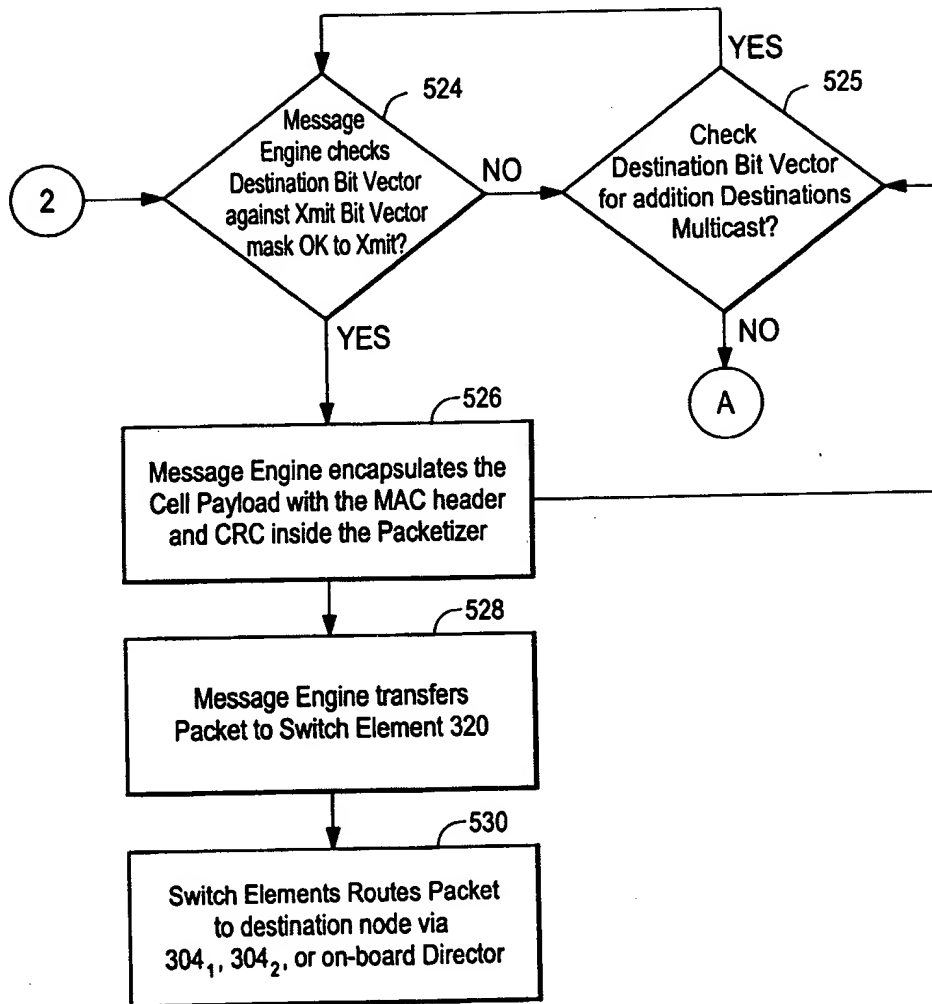


**FIG. 11A**



17/25

Message Bus Send Operation Continued



**FIG. 11B**

Bit Position	1	2	3	4					62	63	64	
	1	0	0	0	—	—	—	—	—	0	0	0

**FIG. 11D**

Bit Position	1	2	3	4	62	63	64
	0	1	0	0	—	—	—

**FIG. 11E**

Bit Position	1	2	3	4					62	63	64	
	0	1	1	0						0	1	1

**FIG. 11F**

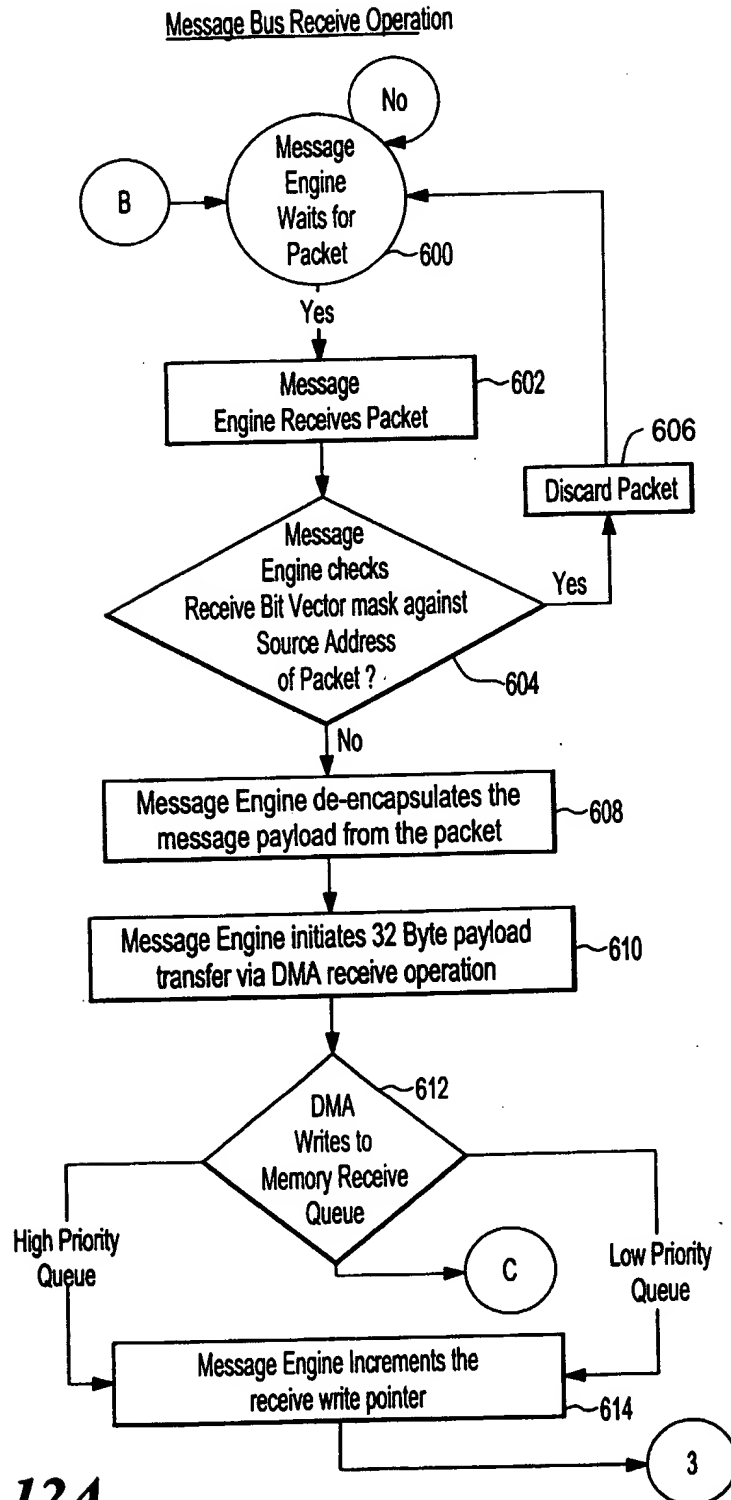
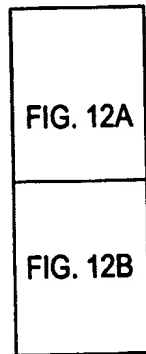
Bit Position	1	2	3	4				62	63	64
	1	1	1	1	—	—	—	1	1	0

**FIG. 11G**

Bit Position	1	2	3	4	62			63	64
	0	1	1	0	—	—	—	—	—

19/25

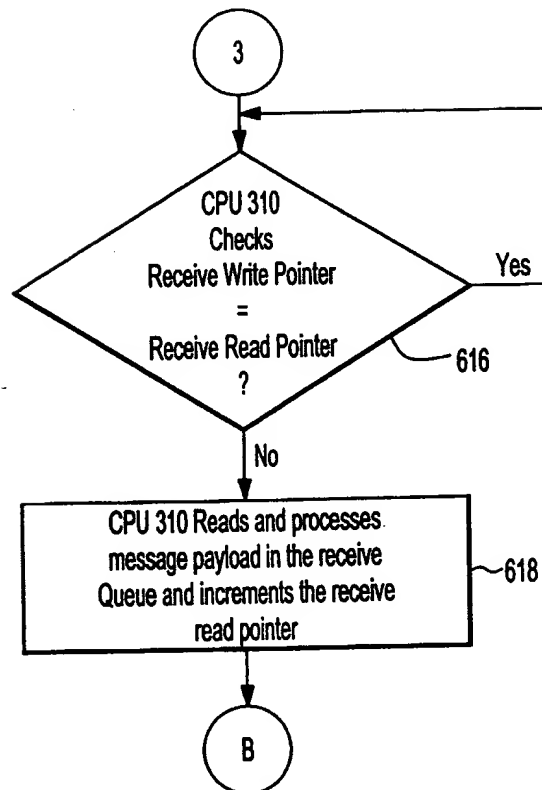
**FIG. 12**



**FIG. 12A**

20/25

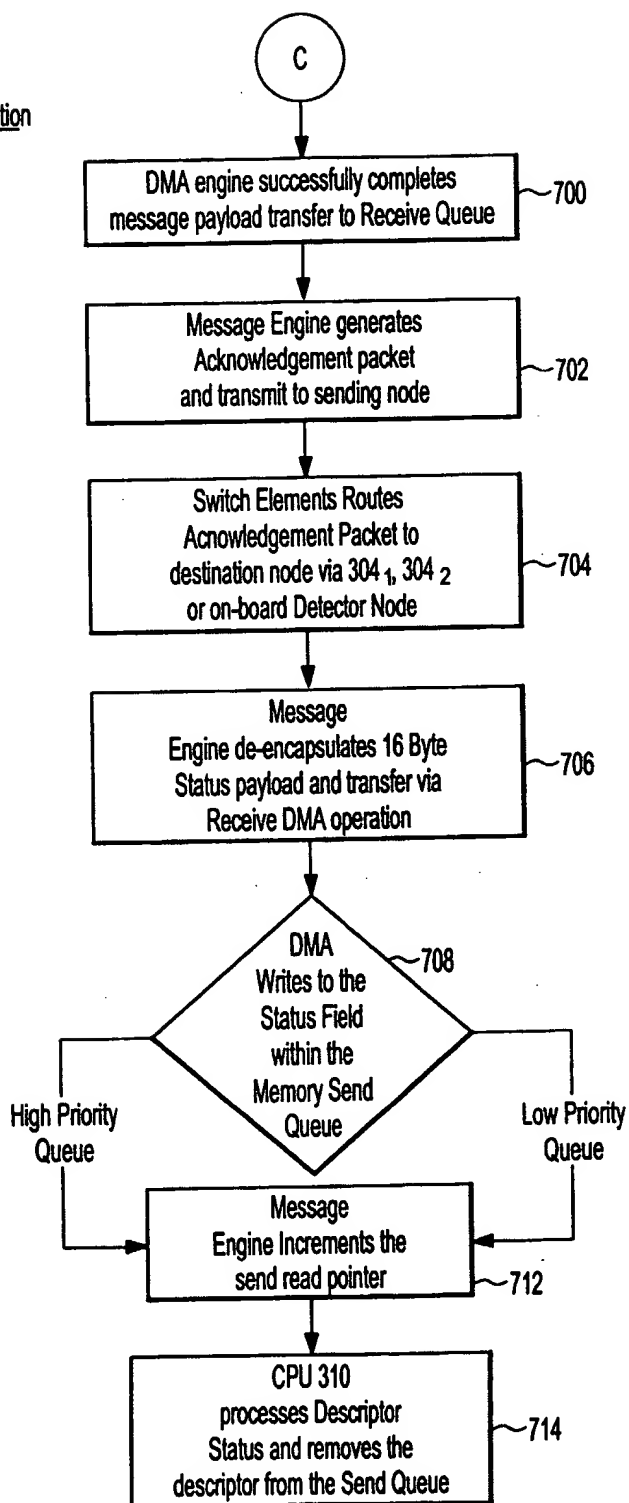
Message Bus Receive Operation Continued



**FIG. 12B**

21/25

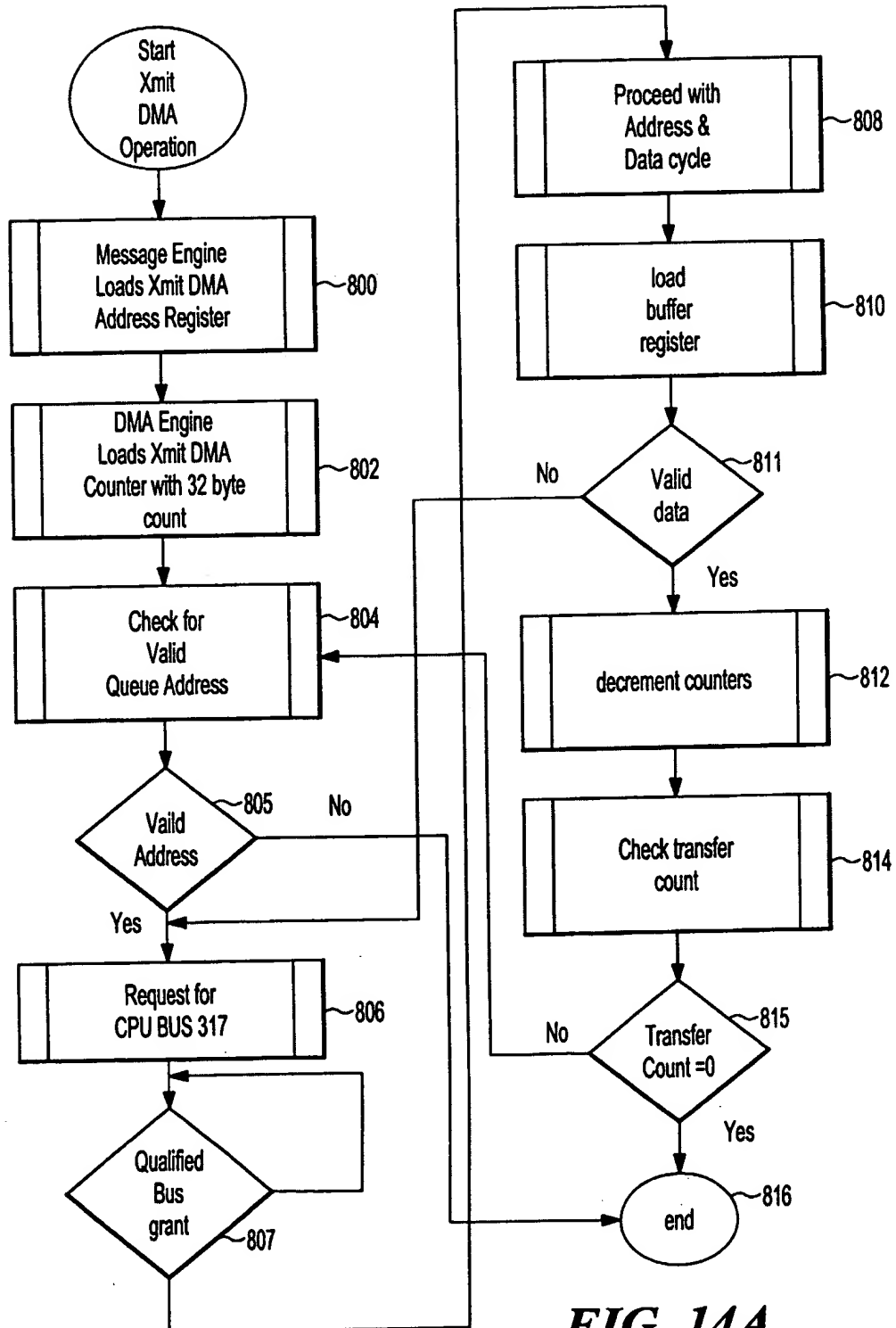
Message Bus  
Acknowledgement Operation



**FIG. 13**

22/25

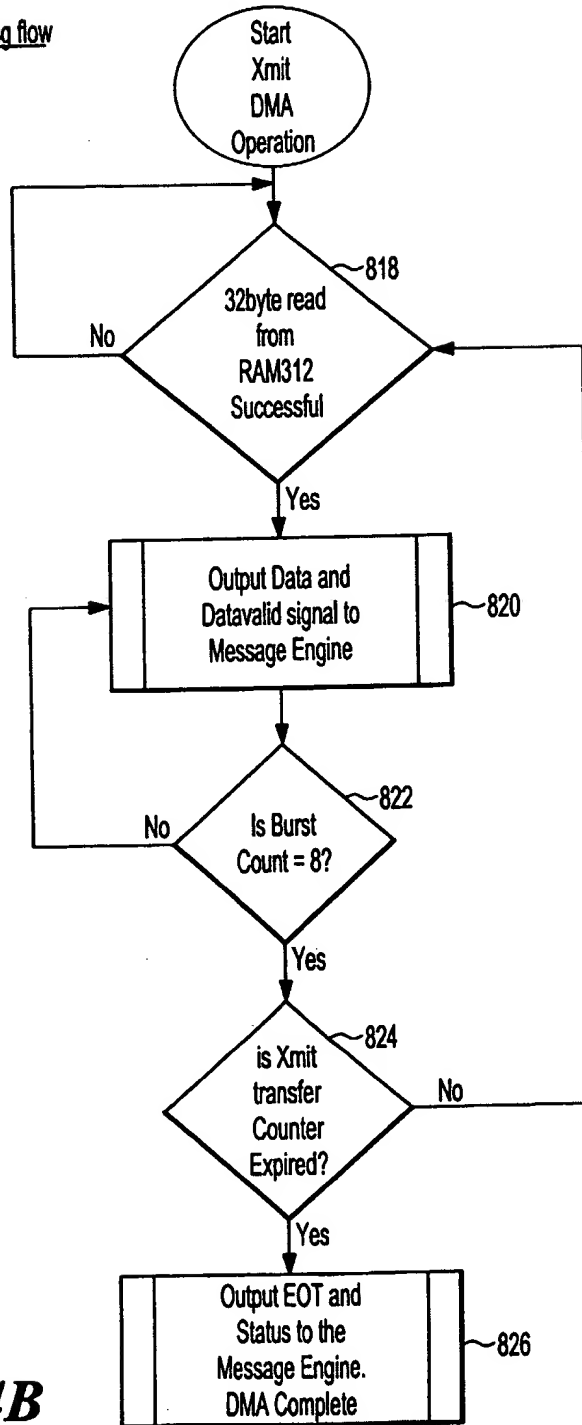
Xmit CPU flow



**FIG. 14A**

23/25

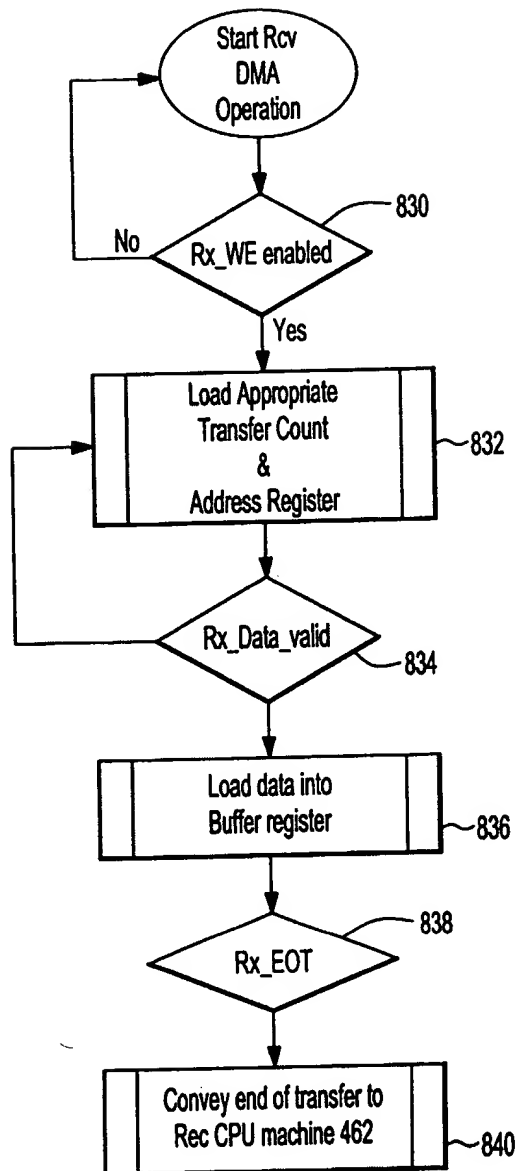
Xmit Msg flow



**FIG. 14B**

24/25

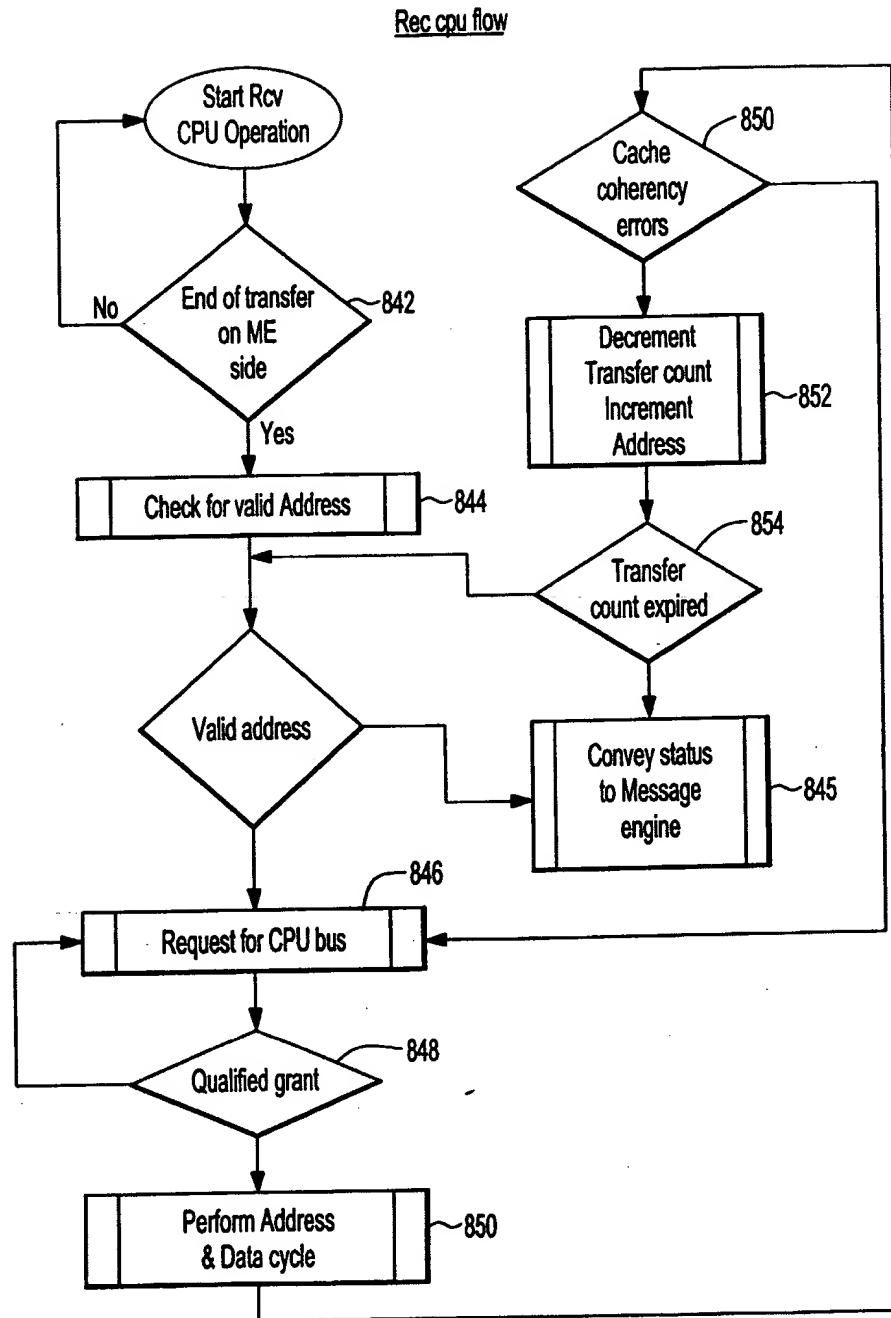
Rec msg flow



**FIG. 15A**



25/25



**FIG. 15B**